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Kindly **add** the following claims:

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1 ~~1 43~~ 42. A method of operation in a semiconductor memory device,
2 wherein the memory device receives an external clock signal and
3 includes an array of memory cells, the method comprises:
4 receiving a first code synchronously with respect to the
5 external clock signal, wherein the first code specifies that a
6 write operation is to be initiated in the memory device
7 receiving a second code synchronously with respect to the
8 external clock signal, wherein the second code specifies that a
9 precharge operation is to be initiated automatically after
10 initiation of the write operation;
11 detecting an external strobe signal, wherein the external
12 strobe signal indicates when to begin sampling data;
13 sampling the data upon detection of the external strobe
14 signal, wherein during the write operation, the memory device
15 writes the data to the array; and
16 initiating the precharge operation automatically after the
17 write operation is initiated.

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1 ~~43~~ 43. The method of claim ~~42~~ wherein a first portion of the
2 data is sampled synchronously with respect to the external clock
3 signal.

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1 ~~44~~ 44. The method of claim ~~43~~ further comprising sampling a
2 second portion of data synchronously with respect to the external
3 clock signal, wherein the first portion of data is sampled during
4 an odd phase of the external clock signal, and the second portion

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5 of data is sampled during an even phase of the external clock
6 signal.

1 ^{4 46} 45. The method of claim ^{3 45} 44 wherein the first and second
2 portions of data are both sampled during the same clock cycle of
3 the external clock signal.

1 ^{5 47} 46. The method of claim ^{1 43} 42 wherein the precharge operation is
2 initiated after the memory device writes the data to the array.

1 ^{6 48} 47. The method of claim ^{1 43} 42 wherein the external strobe signal
is detected by sampling from an external signal line synchronously
with respect to the external clock signal.

1 ^{7 49} 48. The method of claim ^{1 43} 42 further comprising receiving
2 address information synchronously with respect to the external
3 clock signal.

1 ^{8 50} 49. The method of claim ^{7 49} 48, wherein the address information
2 and the data are received from a common set of external signal
3 lines.

1 ^{9 51} 50. The method of claim ^{8 50} 49 wherein the first code, second
2 code and address information are included in a write request
3 packet.

1 ^{10 52} 51. The method of claim ^{1 43} 42 further comprising:
2 receiving a third code synchronously with respect to the

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external clock signal, wherein the third code specifies that the memory device initiate a sense operation; initiating the sense operation; and activating a row of sense amplifiers during the sense operation.

11 ~~53~~
1 ~~52~~. A method of controlling a semiconductor memory device, wherein the memory device includes an array of memory cells, the method comprises:

providing a plurality of control codes to the memory device wherein the plurality of control codes include a first code which specifies that a write operation be initiated in the memory device and a second code which specifies that a precharge operation be initiated automatically after initiation of the write operation; delaying for an amount of time after providing the plurality of control codes; and

issuing an external strobe signal to the memory device after delaying for the amount of time, to signal the memory device to sample data, wherein the data is to be written to the array during the write operation.

12 ~~54~~ 11 ~~53~~
1 ~~53~~. The method of claim ~~52~~ further comprising issuing a first portion of the data and a second portion of the data to the memory device, wherein the first portion of the data is sampled during an odd phase of an external clock signal, and the second portion of the data is sampled during an even phase of the external clock signal.

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1 ~~54~~. The method of claim ~~53~~ wherein the first and second
2 portions of the data are both issued during a first clock cycle of
3 the external clock signal.

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1 ~~55~~. The method of claim ~~52~~ further comprising:
2 issuing additional portions of the data to the memory device;
3 and

✓ 4 issuing the external strobe signal to the memory device to
5 signal the memory device to stop sampling data.

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15 ~~56~~. The method of claim ~~52~~ further comprising providing
2 address information to the memory device.

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16 ~~57~~. The method of claim ~~56~~ wherein the plurality of control
2 codes and the address information are both included in a first
3 packet.

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17 ~~58~~. The method of claim ~~57~~ wherein the data is included in a
2 second packet and wherein the first packet and the second packet
3 are transported over a common set of external signal lines.

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1 ~~59~~. The method of claim ~~52~~ wherein the plurality of control
2 codes includes a third code which specifies that a row of sense
3 amplifiers be activated.

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1 ~~60~~. A synchronous semiconductor memory device having an array
2 which includes a plurality of memory cells, wherein the memory
3 device receives an external clock signal, the memory device
4 comprises:

5 a first input receiver to receive a first code synchronously
6 with respect to the external clock signal, wherein, when the first
7 code specifies a write operation, the memory device samples data
8 upon detection of an external strobe signal;

9 a row of sense amplifiers coupled to the array, to store the
10 data in the array during the write operation; and

11 a second input receiver to receive a second code synchronously
12 with respect to the external clock signal, wherein the second code
13 specifies that precharging the row of sense amplifiers occur
14 automatically after the data is stored in the array.

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15 ~~61~~. The memory device of claim ~~60~~ further comprising a clock
16 generator circuit to receive the external clock signal, wherein the
17 data is sampled synchronously with respect to the external clock
18 signal.

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19 ~~62~~. The memory device of claim ~~60~~ further comprising a
2 plurality of input receiver circuits to sample a first portion of
3 the data and a second portion of the data, wherein the first
4 portion of the data is sampled during an odd phase of an external
5 clock signal, and the second portion of the data is sampled during
6 an even phase of the external clock signal.

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1 63. The memory device of claim 62 wherein the first input
2 receiver and the second input receiver are both included among the
3 plurality of input receiver circuits.

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1 64. The memory device of claim 62 wherein the plurality of
2 input receiver circuits sample additional portions of data until
3 detection of an external termination signal.

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1 65. The memory device of claim 60 wherein the second input
2 receiver samples address information synchronously with respect to
the external clock signal.

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1 66. The memory device of claim 60 further comprising a third
input receiver to sample the external strobe signal.

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1 67. The memory device of claim 60 wherein the first code and
the second code are included in a packet.

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1 68. The memory device of claim 60 further including a third
2 input receiver to receive a third code synchronously with respect
3 to the external clock signal, wherein the third code specifies that
4 the row of sense amplifiers sense the contents of a row of memory
5 cells included in the array.

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1 69. The memory device of claim 68 wherein the data is stored
2 in the row of memory cells included in the array during the write
3 operation.

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1 20. A dynamic random access memory device which receives an
2 external clock signal, the memory device comprises:

3 an array of memory cells;

4 a first input receiver to receive a first code synchronously
5 with respect to the external clock signal, wherein the first code
6 indicates that a write operation be initiated in the memory device;

7 a second input receiver to receive an external strobe signal,
8 wherein receipt of the external strobe signal indicates when the
9 memory device is to begin sampling data, wherein the data is to be
10 stored in the array during the write operation; and

11 a third input receiver to receive a second code which
12 specifies that a row of sense amplifiers be precharged
13 automatically after the data is stored in the array, wherein the
14 second code is received synchronously with respect to the external
15 clock signal.

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16 31. The memory device of claim 30 further comprising a fourth
17 input receiver to receive a third code synchronously with respect
18 to the external clock signal, wherein the third code indicates that
19 the row of sense amplifiers sense the contents of a row of memory
20 cells of the array.

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21 32. The memory device of claim 31 wherein further comprising
22 a plurality of input receivers to receive address information which
23 identifies the row of memory cells, wherein the address information
24 is received synchronously with respect to the external clock

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5 signal.

1 ~~32 73~~ 73. The memory device of claim ~~70~~ 29 24 wherein the third input
2 receiver also receives address information synchronously with
3 respect to the external clock signal.

1 ~~33 74~~ 74. The memory device of claim ~~70~~ 29 24 further comprising a
2 plurality of input receiver circuits to sample a first portion of
3 the data and a second portion of the data, wherein the first
4 portion of the data is sampled during an odd phase of an external
5 clock signal, and the second portion of the data is sampled during
6 an even phase of the external clock signal.

1 ~~34 75~~ 75. The memory device of claim ~~74~~ 33 25 wherein the first and
2 second portions of the data are both sampled during a common clock
3 cycle of the external clock signal.

1 ~~35 76~~ 76. The memory device of claim ~~70~~ 29 24 wherein the first and
2 second codes are included in a packet.

1 ~~36 77~~ 77. The memory device of claim ~~76~~ 35 24 wherein the first and
2 second codes are both included in a first packet and the data is
3 included in a second packet.

1 ~~37 78~~ 78. The memory device of claim ~~77~~ 36 28 wherein the first and
2 second packet are multiplexed over a common set of external signal
3 lines.

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